**IN THE CLAIMS:**

Claims 1 through 15, 23 and 24 are currently pending in the above-identified application. Claims 16 through 22 have been previously cancelled without prejudice or disclaimer. Also, please amend Claims 1, 5, 8 through 14, 23 and 24, as follows:

1. (Currently Amended) A semiconductor integrated circuit, ~~including~~ comprising:

a central processing unit;

a memory including instructions and data; ~~which can enter active state or standby state,~~

a clock generator for generating a plurality of clock signals; and

a bus coupled to said central processing unit and said memory,

wherein said semiconductor integrated circuit has a plurality of operation states including an active state and a standby state,

wherein said semiconductor integrated circuit is instructed as to a transition of the operation state from said active state to said standby state, when said central processing unit executes a predetermined instruction,

wherein said central processing unit can access said memory and said clock generator provides a clock signal to said central processing unit, in said active state,

wherein said central processing unit stops an operation and said clock generator stops generating said clock signals, in said standby state,

wherein said memory has voltage generation circuits for bit lines and source lines with which memory cells are connected, and

wherein said voltage generation circuits make the potential of said bit lines and the potential of said source lines equal to each other in response to an instruction to transition from said active state to said standby state, and produce a potential difference between said bit lines and said source lines in response to an instruction to transition from said standby state to said active state.

2. (Original) The semiconductor integrated circuit according to Claim 1,

wherein said voltage generation circuits make the potential of said source lines equal to the precharge potential of said bit lines in response to an instruction to transition from said active state to said standby state.

3. (Original) The semiconductor integrated circuit according to Claim 1,

wherein said voltage generation circuits make the potential of said bit lines equal to the discharge potential of said source lines in response to an instruction to transition from said active state to said standby state.

4. (Original) The semiconductor integrated circuit according to Claim 2,

wherein said voltage generation circuits discharge the source lines in response to an instruction to transition from said standby state to said active state, and the current supplying capability thereof is varied so that the discharge rate will be enhanced stepwise.

5. (Currently Amended) A semiconductor integrated circuit, ~~which comprises:~~ comprising:

a central processing unit provided a clock signal from a clock generator; [[and]]

a memory accessible from said central processing unit, and said memory can enter an active state or a standby state [[,]]; and

a bus coupled to said central processing unit and said memory,

wherein said semiconductor integrated circuit has a plurality of operation states including said active state and said standby state,

wherein said semiconductor integrated circuit is instructed as to a transition of the operation state from said active state to said standby state, when said central processing unit executes a predetermined instruction,

wherein said central processing unit can access said memory and said clock generator provides said clock signal to said central processing unit, in said active state,

wherein said central processing unit stops an operation and said clock generator stops providing said clock signal to said central processing unit, in said standby state, and

wherein said memory includes memory cells connected with bit lines and source lines, and makes the potential of said bit lines and the potential of said source lines equal to each other in said standby state and can produce a potential difference between said bit lines and said source lines in said active state.

6. (Original) The semiconductor integrated circuit according to Claim 5,

wherein in said standby state, said central processing unit stops instruction execution, and the memory stops access operation.

7. (Original) The semiconductor integrated circuit according to Claim 6,

wherein instructions to transition from said active state to said standby state and instructions to transition from said standby state to said active state are given by an external control signal.

8. (Currently Amended) The semiconductor integrated circuit according to Claim 6,

wherein instructions to transition from said active state to said standby state are given by the central processing unit executing a predetermined instruction, and instructions to transition ~~transitions~~ from said standby state to said active state are given by an interrupt.

9. (Currently Amended) A semiconductor integrated circuit, ~~including~~ comprising:

a memory including instructions and data; ~~which can enter active state or standby state; and~~

a central processing unit which can access said memory; [[,]]

a clock generator for generating a plurality of clock signals; and

a bus coupled to said central processing unit and said memory,

wherein said semiconductor integrated circuit has a plurality of operation modes including an active mode and a standby mode,

wherein said semiconductor integrated circuit is instructed as to a transition of the operation mode from said active mode to said standby mode, when said central processing unit executes a predetermined instruction,

wherein said central processing unit can access said memory and said clock generator provides a clock signal to said central processing unit, in said active mode,

wherein said central processing unit stops an operation and said clock generator stops generating said clock signals, in said standby mode, and

wherein said memory has memory cells connected with bit lines and source lines, and makes the potential of said source lines equal to the precharge potential of said bit lines in said standby ~~state~~ mode and brings the source lines to discharge potential in said active ~~state~~ mode.

10. (Currently Amended) A semiconductor integrated circuit, ~~including~~ comprising:

a memory including instructions and data; ~~which can enter active state or standby state; and~~

a central processing unit which can access said memory; [[,]]

a clock generator for generating a plurality of clock signals and controlled by said central processing unit; and

an internal bus coupled to said central processing unit and said memory,

wherein said semiconductor integrated circuit has a plurality of operation modes including an active mode and a standby mode,

wherein said active mode is changed to said standby mode, when said central processing unit executes a predetermined instruction,

wherein said central processing unit can access said memory and said clock generator provides a clock signal to said central processing unit, in said active mode,

wherein said central processing unit stops an operation and said clock generator stops generating said clock signals, in said standby mode, and

wherein said memory has memory cells connected with bit lines and source lines, and makes the potential of said bit lines equal to the discharge potential of said source lines in said standby state and brings the bit lines to precharge potential in said active state.

11. (Currently Amended) The semiconductor integrated circuit according to Claim 9,

wherein the central processing unit is brought into a state in which instruction execution is stopped in parallel with said memory entering said standby mode ~~state~~, and said standby mode ~~state~~ and said state in which instruction execution is stopped can be released by an interrupt or external control signal.

12. (Currently Amended) A semiconductor integrated circuit, comprising ~~including~~:

a central processing unit; [[and]]

a memory accessible from said central processing unit [[,]] ; and

a bus coupled to said central processing unit and said memory,

wherein said semiconductor integrated circuit has a plurality of operation states including a first state and a second state,

wherein said semiconductor integrated circuit changes said first state to said

second state, when said central processing unit executes a predetermined instruction,

wherein said memory has bit lines connected with a first circuit, source lines connected with a second circuit, and memory cells which are connected with said bit lines and said source lines and whose select terminals are connected with word lines,

wherein said semiconductor integrated circuit can select said first state in which the access operation of said memory and the data processing operation of the central processing unit are enabled, and said second state in which the access operation of said memory and the data processing operation of the central processing unit are disabled, and

wherein in said first state, said first circuit charges the bit lines and said second circuit discharges the source lines, and in said second state, said first circuit charges the bit lines and said second circuit charges the source lines.

13. (Currently Amended) A semiconductor integrated circuit, comprising ~~including~~:

a central processing unit; [[and]]

a memory accessible from said central processing unit [[,]]; and

a clock generator for generating a plurality of clock signals,

wherein said semiconductor integrated circuit has a plurality of operation states including a first state and a second state,

wherein said semiconductor integrated circuit changes said first state to said second state, when said central processing unit executes a predetermined instruction in said first state,

wherein said clock generator provides a clock signal to said central processing unit in said first state, and said clock generator stops providing the clock signal in said second state,

wherein said memory has bit lines connected with a first circuit, source lines connected with a second circuit, and memory cells which are connected with said bit lines and said source lines and whose select terminals are connected with word lines,

wherein said semiconductor integrated circuit can select said first state in which the access operation of said memory and the data processing operation of the central processing unit are enabled, and said second state in which the access operation of said memory and the data processing operation of the central processing unit are disabled, and

wherein in said first state, said first circuit charges the bit lines and said

second circuit discharges the source lines, and in said second state, said first circuit discharges the bit lines and said second circuit discharges the source lines [[line]].

14. (Currently Amended) The semiconductor integrated circuit according to Claim 13,

wherein the ultimate level of the [[said]] discharge is equal to the ground potential of the circuit and the unselect level of said word lines is equal to the ground potential of the circuit.

15. (Original) The semiconductor integrated circuit according to Claim 13,

wherein in said first state, said first circuit stops the operation of charging the bit lines through which readout is carried out.

16-22. (Cancelled)

23. (Currently Amended) A semiconductor integrated circuit, comprising ~~which includes~~:

a central processing unit;

a clock generator for generating a plurality of clock signals; and

a memory including memory cells connected with bit lines and source lines [[;]] and voltage generation circuits for the bit lines and the source lines, ~~and is selectively brought into standby state or active state,~~

wherein said semiconductor integrated circuit has a plurality of operation states including an active state and a standby state,

wherein said semiconductor integrated circuit changes said active state to said standby state, when said central processing unit executes a predetermined instruction in said active state,

wherein said clock generator provides a clock signal to said central processing unit in said active state, and said clock generator stops providing the clock signal in said standby state, and

wherein in said active state, said voltage generation circuits produce a predetermined potential difference between said bit lines and said source lines, and in said standby state, said voltage generation circuits reduce the potential difference between said bit lines and said source lines of said memory to a value smaller than the potential difference in said active state.

24. (Currently Amended) The semiconductor integrated circuit according to Claim 23,

wherein in the process of the semiconductor integrated circuit transitioning from said standby state to said active state, said voltage generation circuits produce said predetermined potential difference between said bit lines and said source lines by source line discharge, and enhance the discharge rate stepwise.